

SEMITRONICS CORP.

64 Commercial Street, Freeport, N.Y. 11520
Phone: (516) 623-9400 • Fax. (516) 623-6954

SEFN9140

P-Channel MOSFET

FEATURES

- Surface Mount Case
- Hermetically Sealed Package
- Repetitive Avalanche Rating
- Dynamic dv/dt Rating
- Ease of Paralleling
- MIL STX Screening Available

APPLICATIONS

- High Reliability Power Supplies
- Switch Mode Power Supplies
- Battery Back-Up Supplies
- High Speed Power Switching
- Inverters & Choppers

DESCRIPTION

The SEFN9140 is a -18 Amp, -100 volts, 0.20 ohms, Power Mosfet packaged in an electrically isolated surface mount SMD-1 hermetic package.

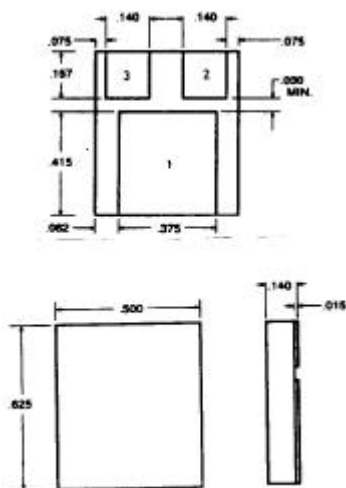
Geared for military Hi-Rel SMD production lines
Special Pin-Outs Available
Add STX suffix for Military Screening

PACKAGE



SMD-1

CASE OUTLINE



Pad 1: D Pad 2: G Pad 3: S

Absolute Maximum Ratings

Parameter	Maximum	Units
Continuous Drain Current I_p @ $T_c = 25^\circ C$, $V_{GS} @ -10V$	-18	A
Continuous Drain Current I_p @ $T_c = 100^\circ C$, $V_{GS} @ -10V$	-11	A
Pulse Drain Current I_{DM}	-72	A
Power Dissipation $P_D @ T_c = 25^\circ C$	125	W
Linear Derating Factor	1.0	W/ $^\circ C$
Gate-to-Source Voltage V_{GS}	± 20	V
Peak Diode Recovery dv/dt	-5.0	V/ns
Operating & Storage Temperature T_j & T_{STG}	-55 to 150	$^\circ C$

Static @ T_j = 25°C (unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Breakdown Voltage V _{(BR)DSS}	-100	—	—	V	V _{GS} = 0V, I _D = -1.0mA
Static Drain to Source On-Resistance R _{DS(on)}	—	—	0.20 0.22	Ω	V _{GS} = -10V, I _D = -11A V _{GS} = -10V, I _D = -18A
Gate Threshold Voltage V _{GS}	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -250uA
Drain-to-Source Leakage Current I _{DSS}	—	—	-25	uA	V _{DS} = 0.8 x Max rating, V _{GS} = 0V
	—	—	-250		V _{DS} = 0.8 x Max Rating, V _{GS} = 0V, T _J = 125°C
Gate-to-Source Forward Leakage I _{GSS}	—	—	-100	nA	V _{GS} = -20V
Gate-to-Source Reverse Leakage I _{GSS}	—	—	100		V _{GS} = 20V

Dynamic @ T_j = 25°C (unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Conditions
Forward Transconductance g _{fs}	6.2	—	—	S	V _{DS} = >-15V, I _{DS} = -11A
Total Gate Charge Q _g	—	—	60	nC	I _D = 188A V _{DS} = 0.5 x Max Rating V _{GS} = -10V
Gate-to-Source Charge Q _{gs}	—	—	13		
Gate-to-Drain ("Miller") charge Q _{gd}	—	—	35.2		
Turn-on-Delay Time t _{d(on)}	—	—	35	ns	V _{DD} = -50V I _D = -18A R _G = 9.1 Ohms V _{GS} = -10V
Rise Time t _r	—	—	85		
Turn-Off-Delay Time t _{d(off)}	—	—	85		
Fall time t _f	—	—	65		
Input Capacitance C _{iss}	—	1400	—	pF	V _{GS} = 0V V _{DS} = -25V f = 1.0 MHz
Output Capacitance C _{oss}	—	600	—		
Reverse Transfer Capacitance C _{rss}	—	200	—		
Internal Drain Inductance L _D	—	4.0	—	nH	Measured from the center of the drain pad to the center of the source pad.
Internal Source Inductance L _S	—	4.0	—		

Avalanche Characteristics

Parameter		Typ.	Max.	Units
Single Pulse Avalanche Energy	E_{AS}	—	500	mJ
Avalanche Current	I_{AR}	—	-18	A
Repetitive Avalanche Energy	E_{AR}	—	12.5	mJ

Thermal Resistance

Parameter		Typ.	Max.	Units
Junction-to-case	$R_{\theta JC}$	—	1.0	°C/W
Junction-to-PC Board (Copper Clad PCB)	$R_{\theta J-PCB}$	4.0	—	

Diode Characteristics

Parameter		Min.	Typ.	Max.	Units	Conditions
Continuous Source Current	I_S	—	—	-18	A	
Pulsed Source Current	I_{SM}	—	—	-72		
Diode Forward Voltage	V_{SD}	—	—	-5.0	V	$T_j = 25^\circ\text{C}$, $I_S = -18\text{A}$, $V_{GS} = 0\text{V}$
Reverse Recovery Time	t_{rr}	—	—	280	ns	$T_j = 25^\circ\text{C}$, $I_F = -18\text{A}$ $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = -30\text{V}$
Reverse Recovery Charge	Q_{rr}	—	—	2.9	uC	
Forward Turn-on Time	t_{on}	Intrinsic turn-on time is negligible				

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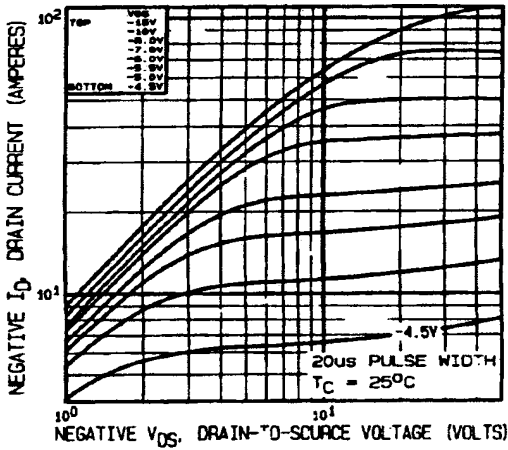


Fig 1. Typical Output Characteristics

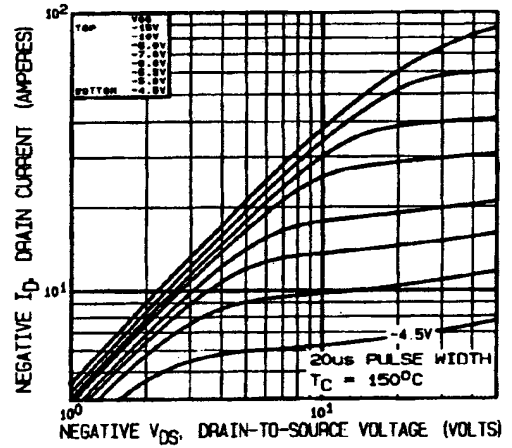


Fig 2. Typical Output Characteristics

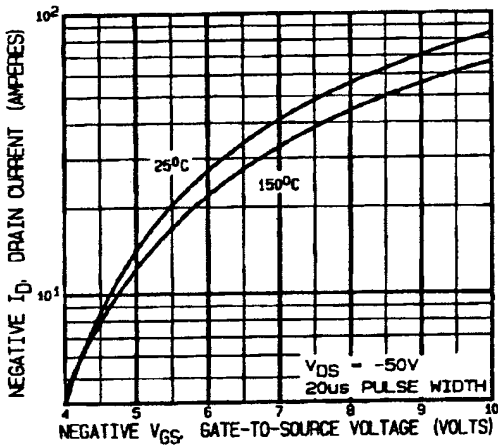


Fig 3. Typical Transfer Characteristics

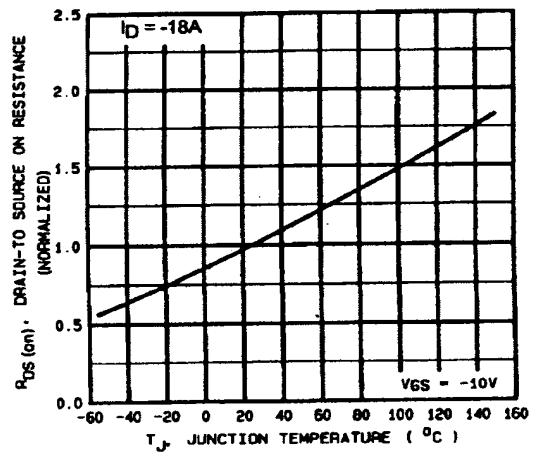


Fig 4. Normalized On-Resistance Vs. Temperature

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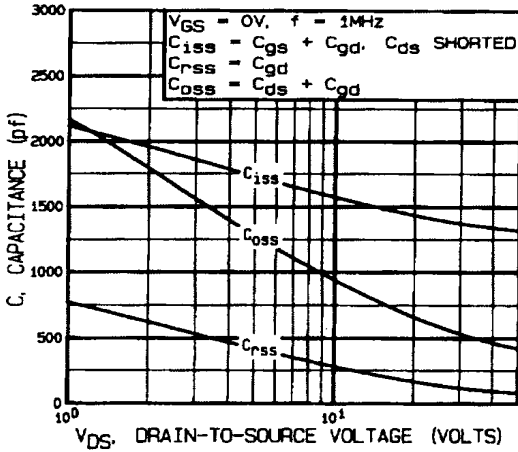


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

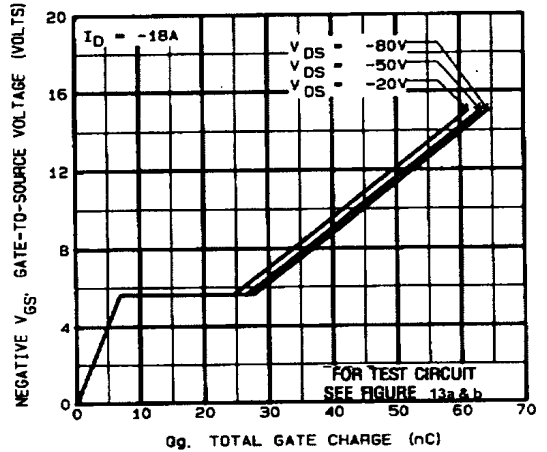


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

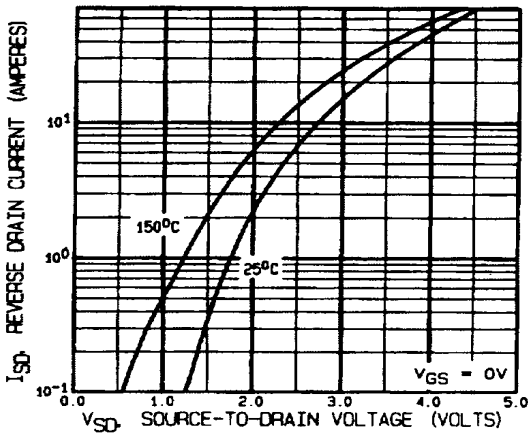


Fig 7. Typical Source-Drain Diode Forward Voltage

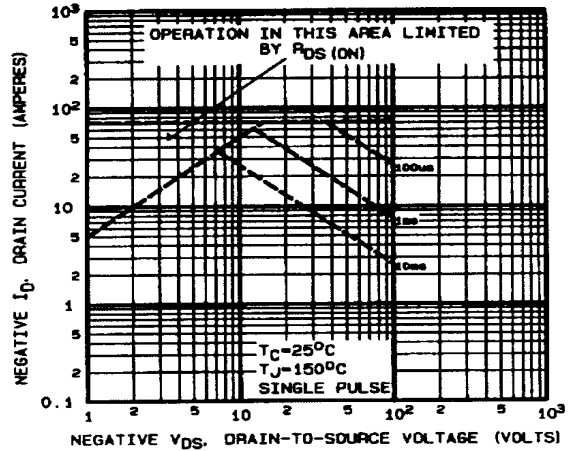


Fig 8. Maximum Safe Operating Area

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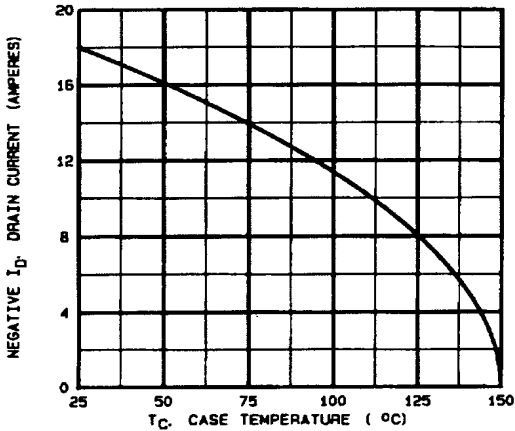


Fig 9. Maximum Drain Current Vs. Case Temperature

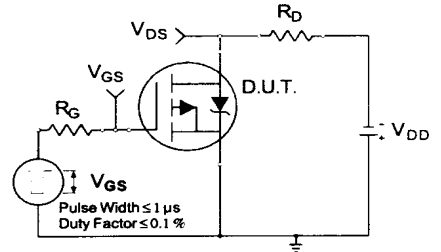


Fig 10a. Switching Time Test Circuit

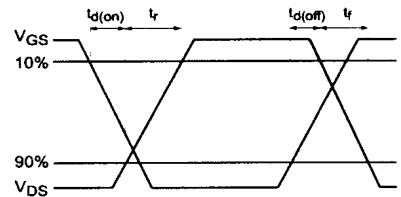


Fig 10b. Switching Time Waveforms

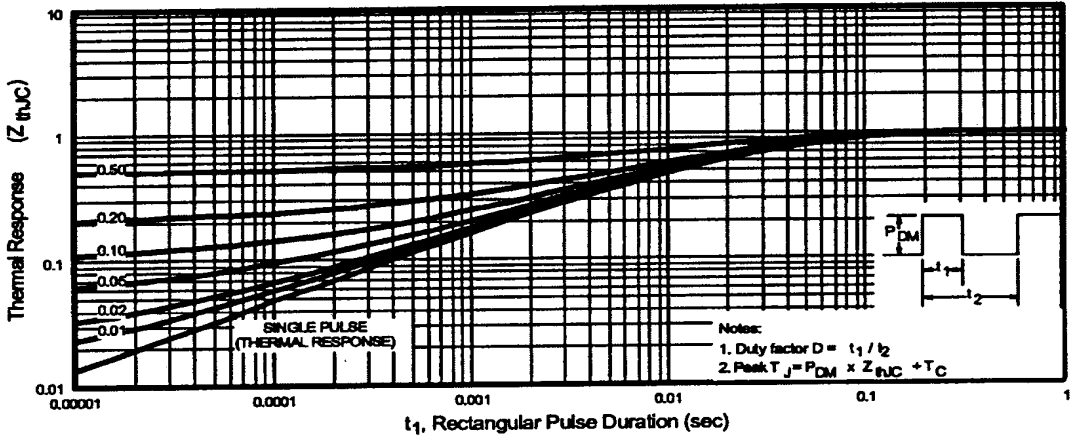


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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